CLAIMS

The invention claimed is:

1. A method of fabricating an interconnect for a semiconductor component, comprising:

providing a semiconductor component;

forming an opening which extends entirely through the component, the opening having sidewalls;

depositing a first material along the sidewalls of the opening, the depositing being conducted at a temperature of less than or equal to about 200°C; and

plating a second material within the opening and over the first material.

2. The method of claim 1 wherein the depositing comprises one or both of ALD and CVD.

3. The method of claim 1 wherein the depositing comprises one or both of ALD and CVD, and wherein the depositing utilizes multiple cycles which individually form less than or equal to about 10Å of the first material.

4. The method of claim 3 wherein the first material is formed to a thickness of at least about 100Å.

5. The method of claim 3 wherein the first material is formed to a thickness of from about 100Å to about 300Å.

6. The method of claim 1 wherein the component comprises a semiconductor material wafer.

7. The method of claim 1 wherein the component comprises a monocrystalline silicon wafer.

8. The method of claim 1 wherein the opening has a length through the component and a maximum dimension orthogonal to the length of less than or equal to about 100 microns.

9. The method of claim 1 wherein the first material is an electrically-conductive material.

10. The method of claim 1 wherein the first material comprises a metal nitride.

11. The method of claim 1 wherein the first material consists essentially of a metal nitride.

12. The method of claim 1 wherein the first material consists of a metal nitride.

13. The method of claim 1 wherein the first material comprises one or more of titanium nitride, tungsten nitride, tantalum nitride and hafnium nitride.

14. The method of claim 1 wherein the first material consists essentially of one or more of titanium nitride, tungsten nitride, tantalum nitride and hafnium nitride.

15. The method of claim 1 wherein the first material consists of one or more of titanium nitride, tungsten nitride, tantalum nitride and hafnium nitride.

16. The method of claim 1 wherein the plating is electroless plating.

17. The method of claim 16 wherein the second material comprises nickel.

18. The method of claim 16 wherein the first material comprises a metal nitride, and further comprising activating the metal nitride with one or both of Hf and Pd prior to the electroless plating.

19. The method of claim 18 wherein the activating the metal nitride forms a layer comprising one or both of Hf and Pd over the metal nitride, and wherein the layer comprising one or both of Hf and Pd has a thickness of from about 1 micron to about 7 microns.

20. The method of claim 19 wherein the layer comprising one or both of Hf and Pd has a thickness of at least about 5 microns.

21. The method of claim 1 wherein the component comprises a first side and an opposing second side, wherein the opening extends from the first side to the second side, the method further comprising forming a conductive-material pad over the first side, and wherein the opening is formed through the conductive-material pad.

22. The method of claim 1 wherein the second material is a solder-wetting material, and further comprising forming solder within the opening and along the solder-wetting material.

23. The method of claim 22 wherein the solder-wetting material comprises nickel.

24. A method of fabricating an interconnect for a semiconductor component, comprising:

providing a semiconductor component;

forming an opening which extends entirely through the component, the opening having sidewalls;

depositing a metal nitride along the sidewalls of the opening, the depositing being conducted in a reaction chamber utilizing:

a first precursor containing the metal of the metal nitride;

a second precursor containing the nitrogen of the metal nitride; and

at least one cycle in which the first and second precursors are in the reaction chamber at different and substantially non-overlapping time intervals relative to one another; and

plating a second material within the opening and over the metal nitride.

25. The method of claim 24 wherein the plating is electroless plating.

26. The method of claim 24 wherein the component comprises a semiconductor material wafer.

27. The method of claim 24 wherein the component comprises a monocrystalline silicon wafer.

28. The method of claim 24 wherein the opening has a length through the component and a maximum dimension orthogonal to the length of less than or equal to about 100 microns.

29. The method of claim 24 wherein a temperature of the component during the at least one cycle is less than or equal to about 200°C.

30. The method of claim 24 wherein a temperature of the component during the at least one cycle is less than or equal to about 160°C.

31. The method of claim 24 wherein the metal nitride is titanium nitride, tungsten nitride, tantalum nitride or hafnium nitride.

32. The method of claim 24 wherein the metal nitride is titanium nitride.

33. The method of claim 32 wherein the first precursor is $TiCl_4$ and the second precursor is NH_3.

34. The method of claim 32 wherein the first precursor is TDMAT and the second precursor is NH_3.

35. The method of claim 34 wherein the cycle utilizes, in the following sequential order, a first pulse of the TDMAT into the reaction chamber, a substantial purge of the TDMAT from the reaction chamber, and a second pulse of the NH_3 into the reaction chamber.

36. The method of claim 35 wherein the first pulse is for a time of about 1 second, the purge is for a time of about 10 seconds and utilizes a purge gas which is inert relative to reaction with the TDMAT and the component, and the second pulse is for a time of about 4 seconds.

37. The method of claim 24 wherein, during each of the at least one cycles, the first precursor is introduced into the reaction chamber before the second precursor.

38. The method of claim 24 wherein each of the at least one cycles individually forms a layer of the metal nitride that is less than or equal to about 10Å thick.

39. The method of claim 38 wherein enough of the cycles are utilized so that the depositing forms the metal nitride to be at least about 100Å thick.

40. The method of claim 38 wherein enough of the cycles are utilized so that the depositing forms the metal nitride to be from about 100Å thick to about 300Å thick.

41. The method of claim 24 wherein the second material is a solder-wetting material, and further comprising forming solder within the opening and along the second material.

42. The method of claim 41 wherein the second material comprises nickel.

43. A method of fabricating an interconnect for a semiconductor component, comprising:

providing a semiconductor component, the component comprising a monocrystalline semiconductor material having a pair of opposing sides, the component comprising a front side outwardly of one of the opposing sides of the monocrystalline semiconductor material and a back side outwardly of the other of the opposing sides of the monocrystalline semiconductor material, the component further comprising a conductive-material layer proximate the front side;

forming an opening which extends from the front side to the back side and thus extends entirely through the semiconductor component, the opening having sidewalls and extending through the conductive-material layer;

depositing a first material along the sidewalls of the opening to narrow the opening, the depositing utilizing one or more cycles of a process which forms less than or equal to about 10Å of the first material per cycle and which exposes the component to a temperature of less than or equal to about 200°C;

forming a solder-wetting material within the opening and along the first material; and

forming solder along the solder-wetting material to fill the opening with solder; the solder within the opening electrically connecting with the conductive-material layer.

44. The method of claim 43 wherein the first material is a metal nitride and wherein the process is conducted in a reaction chamber utilizing:

a first precursor containing the metal of the metal nitride;

a second precursor containing the nitrogen of the metal nitride; and

provision of the first and second precursors in the reaction chamber at different and substantially non-overlapping time intervals relative to one another.

45. The method of claim 44 wherein the metal nitride is titanium nitride, tungsten nitride, tantalum nitride or hafnium nitride.

46. The method of claim 44 wherein the metal nitride is titanium nitride.

47. The method of claim 46 wherein the first precursor is $TiCl_4$ and the second precursor is NH_3.

48. The method of claim 46 wherein the first precursor is TDMAT and the second precursor is NH_3.

49. The method of claim 48 wherein the process utilizes, in the following sequential order, a first pulse of the TDMAT into the reaction chamber, a substantial purge of the TDMAT from the reaction chamber, and a second pulse of the NH_3 into the reaction chamber.

50. The method of claim 43 wherein the semiconductor component comprises a first insulative-material layer over the conductive-material layer and a second insulative-material layer over the first insulative-material layer, and wherein the second insulative-material layer has a surface corresponding to the front side of the semiconductor component.

51. The method of claim 50 wherein the first insulative-material layer comprises polyimide and the second insulative-material layer comprises silicon dioxide.

52. The method of claim 43 wherein a gap extends through the conductive-material layer, and wherein the forming the opening comprises:

forming a first opening within the gap, the first opening not extending to the conductive-material layer; and

extending a portion of the first opening to the conductive-material layer.

53. The method of claim 52 wherein the extending occurs prior to the forming of the solder-wetting material.

54. The method of claim 52 wherein the forming of the solder-wetting material comprises electroless plating of the solder-wetting material.

55. The method of claim 54 wherein the first material comprises a metal nitride, and further comprising activating the metal nitride with one or both of Hf and Pd prior to the electroless plating.

56. The method of claim 55 wherein the activating occurs prior to the extending.

57. The method of claim 55 wherein the activating occurs after the extending.

58. The method of claim 54 wherein the extending occurs after the electroless plating.

59. The method of claim 52 further comprising forming an electrically-insulative material over the conductive material and within the gap in the layer of conductive material, wherein the first opening extends through the electrically-insulative material, and wherein the extending comprises removing at least a portion of the electrically-insulative material.

60. The method of claim 59 wherein the electrically-insulative material comprises a silicon dioxide-containing layer.

61. The method of claim 60 further comprising forming a polymide-containing layer over the layer of conductive material, and wherein the silicon dioxide-containing layer is over the polymide-containing layer.

62. The method of claim 43 wherein the first material comprises a metal nitride.

63. The method of claim 43 wherein the first material consists essentially of a metal nitride.

64. The method of claim 43 wherein the first material consists of a metal nitride.

65. The method of claim 43 wherein the first material comprises one or more of titanium nitride, tungsten nitride, tantalum nitride and hafnium nitride.

66. The method of claim 43 wherein the first material consists essentially of one or more of titanium nitride, tungsten nitride, tantalum nitride and hafnium nitride.

67. The method of claim 43 wherein the first material consists of one or more of titanium nitride, tungsten nitride, tantalum nitride and hafnium nitride.

68. The method of claim 43 wherein the forming of the solder-wetting material comprises electroless plating of the solder-wetting material.

69. The method of claim 68 wherein the first material comprises a metal nitride, and further comprising activating the metal nitride with one or both of Hf and Pd prior to the electroless plating.

70. The method of claim 43 wherein the depositing forms the first material along the back side of the semiconductor wafer, and further comprising removing the first material from over the back side of the semiconductor wafer.

71. The method of claim 70 wherein the forming of the solder-wetting material comprises electroless plating of the solder-wetting material, and wherein the removing occurs prior to the electroless plating.

72. The method of claim 71 wherein the first material comprises a metal nitride, and further comprising activating the metal nitride with one or both of Hf and Pd prior to the electroless plating.

73. The method of claim 72 wherein the activating occurs prior to the removing.

74. The method of claim 72 wherein the activating occurs after the removing.

75. The method of claim 70 wherein the forming of the solder-wetting material comprises electroless plating of the solder-wetting material, and wherein the removing occurs after the electroless plating.